aperture ratio.

b3 end

The data bus line and source/drain electrodes are formed by sputtering and patterning a metal such as Al, Mo, Cr, Ta, or Al alloy, etc. At this time, a storage electrode is formed to overlap the gate bus line 1 at the same time, the storage electrode makes a storage capacitor with gate bus line 1.

Page 12, between lines 2 and 11, please delete the current paragraph and insert therefor the following one paragraph.

B4

One the second substrate 33, a light shielding layer 25 is formed to shield any light leakage from gate and data bus lines 1, and the TFT. A color filter layer 23 is formed R, G, B (red, green blue) elements which are repeated. A common electrode 17 is formed with ITO on the color filter layer 23 as the pixel electrode 13, and a dielectric frame 53 is formed by deposition photosensitive material in a region other than a region where the pixel electrode 13 is formed and patterning in various shapes using photolithography.

REMARKS

By this Amendment, Applicants amend the specification to correspond with the Figures and obviate the objection to the drawings. Claims 1-37 stand rejected by the Office Action of October 17, 2002 as being unpatentable over Applicants admitted prior art in view of U.S. Patent No. 6,344,883 to Yamada (hereinafter the '883 patent). Reexamination and reconsideration of the application, are respectfully requested.

Claims 1-37 are rejected under 35 U.S.C. §103 as being unpatentable over Applicants admitted prior art in view of the '883 patent.

In rejecting the claims, the Examiner has applied the '883 patent and asserts:

"[The 883 patent] discloses . . . a dielectric frame, 36, (OMR83 col. 26, lines 45-62) in a region other than a region where said pixel (pixel region in 10C)

electrode is formed on one or both of the substrates (col. 20, lines 8-12), said dielectric frame(s) distorting electric field applied to said liquid crystal layer (inherent to dielectric material, OMR83), and an alignment layer, 38a and 38b, on at least one substrate between said first and second substrates." (Office Action at pg. 4).

Applicants respectfully disagree and reconsideration is requested.

In the Examiner's assertions that Yamada '883 discloses among other things, a dielectric frame, 36 (OMR83), a careful examination of Yamada reveals that OMR83 is in fact a photoresist. It seems that the Examiner is taking Official Notice that a photoresist is a dielectric. Applicant respectfully submits, the Examiner may take official notice of facts outside of the record, which are capable of instant and unquestionable demonstration as being "well-known" in the art. However, as set forth in MPEP 2144.03, if an applicant traverses an assertion made by an Examiner while taking Official Notice, the Examiner should cite a reference in support of their assertion. Accordingly, Applicants respectfully traverses the use of the Official Notice rejection in the present Office Action.

Applicant submits that Claims 1-37 are allowable over the cited references in that each of these claims recites a combination of elements, including, for example, a second "a dielectric protrusion between the first dielectric frame and the second dielectric frame" as cited in independent claim 1, and similarly "a third dielectric protrusion between the first dielectric protrusion and second dielectric protrusion" as recited in independent claim 9, and similarly "a third insulating protrusion between the first and second insulating protrusions and acting as a spacer between the first and second substrates" as recited in independent claim 20. Accordingly, Applicants respectfully submit that independent claims 1, 9 and 20, and claims 2-8, 10-19 and 21-37, which depend from independent claims 1, 9 and 20, are allowable over the cited references.

Thus, and in view of the asserted disclosure in Yamada, the cited references, singly or in combination, fail to teach or suggest the features of the claimed invention.

Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 1-37 under § 103 in view of Applicants admitted prior art and the '883 patent.

Thus, Applicants respectfully submit that claims 1-37 are allowable over the cited references. Applicants believe that the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned representative at (202) 496-7500.

If these pages are not timely filed by the U.S. Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or for any fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to Deposit Account No. 50-0911.

Dated: January 14, 2003

Respectfully submitted,

By Rebecca Goldman Rudich
Rebecca Goldman Rudich
Registration No.: 41,786

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Attachment:
Appendix Showing Changes to the Specification Made Thereto

APPENDIX SHOWING CHANGES TO THE SPECIFICATION MADE THERETO

Pages 8-9, between page 8, line 15 and page 9, line 3, please delete the two paragraphs and replace therefor with the following two paragraphs.

As shown in the above figures, the multi-domain liquid crystal display device according to the present invention comprises first and second substrates 31, 33, a plurality of gate and data bus lines 1, ~~3~~ arranged in the perpendicular and horizontal directions on the first substrate to divide the first substrate into a plurality of pixel regions.

The TFT is formed on each pixel region on the first substrate 31 and comprises a gate electrode 11, a gate insulator 35, a semiconductor layer ~~5~~, a ohmic contact layer, a source electrode ~~7~~, a drain electrode ~~9~~, etc.

Page 9, between lines 8 and 13, please delete the one paragraph and replace therefore with the following one paragraph.

And, on the second substrate 33, a light shielding layer 25 is formed to shield light leakage from the gate bus line 1, data bus line ~~3~~, and TFT. A color filter layer 23 is on light shielding layer 25. A common electrode 17 is on color filter layer 23. And a liquid crystal layer is between the first and second substrates 31 and 33.

Pages 10-11, between page 10, line 11 and page 11, line 16 please delete the current four paragraphs and replace therefor with the following four paragraphs.

To manufacture the LCD, in each pixel region on the first substrate 31, a TFT is formed comprising a gate electrode ~~11~~, a gate insulator 35, a semiconductor layer ~~5~~, an ohmic contact layer 6 and source/drain electrodes ~~7, 9~~.

At this time, a plurality of gate bus lines 1 and a plurality of data bus lines ~~3~~ are formed to divide the first substrate 31 into a plurality of pixel regions.

The gate electrode ~~11~~ and the gate bus line 1 are formed by sputtering and patterning a metal such as Al, Mo, Cr, Ta, or Al alloy, the combination of the metals etc. The gate insulator 35 is formed by depositing SiN_x or SiO_x using PECVD (Plasma Enhancement Chemical Vapor Deposition) thereon.

The semiconductor layer 5 and the ohmic contact layer ~~6~~ are formed by depositing with PECVD, and patterning amorphous silicon (a-Si) and doped amorphous silicon (n^+ a- Si), respectively. Also, the gate insulator 35 can be formed by depositing SiNx, SiOx, a-Si and n^+ a-Si continuously, and then the semiconductor layer ~~5~~ and the ohmic contact layer can be formed by patterning a-Si and n+ a-Si. Further the gate insulator 35 can be formed with BCB (BenzoCycloButene), acrylic resin or polyimide based material so as to improve aperture ratio.

The data bus line ~~3~~ and source/drain electrodes ~~7, 9~~ are formed by sputtering and patterning a metal such as Al, Mo, Cr, Ta, or Al alloy, etc. At this time, a storage electrode is formed to overlap the gate bus line 1 at the same time, the storage electrode makes a storage capacitor with gate bus line 1.

Page 12, between lines 2 and 11, please delete the current paragraph and insert therefor the following one paragraph.

One the second substrate 33, a light shielding layer 25 is formed to shield any light leakage from gate and data bus lines 1, ~~3,~~ and the TFT. A color filter layer 23 is formed R, G, B (red, green blue) elements which are repeated. A common electrode 17 is formed with ITO on the color filter layer 23 as the pixel electrode 13, and a dielectric frame 53 is formed by deposition photosensitive material in a region other than a region where the pixel electrode 13 is formed and

patterning in various shapes using photolithography.